Claims

What is claimed is:

1. A high voltage gallium nitride (GaN) transistor structure comprising:

a) a substrate;

b) a plurality of epitaxial layers deposited on the substrate and comprising:

i) a transitional layer deposited above the substrate;

ii) a sub-buffer layer deposited above the transitional layer and adapted to prevent electrons from entering the transitional layer and the substrate during high voltage operation; and

iii) a GaN buffer layer deposited above the sub-buffer layer; and

c) electrical contacts deposited on the plurality of epitaxial layers, thereby forming a high electron mobility transistor.

2. The structure of claim 1 wherein the sub-buffer layer is essentially aluminum nitride.

3. The structure of claim 1 wherein the plurality of epitaxial layers further comprise a Schottky layer deposited above the GaN buffer layer.

4. The structure of claim 3 wherein the Schottky layer is essentially aluminum gallium nitride.

5. The structure of claim 3 wherein the plurality of epitaxial layers further comprise a GaN termination layer deposited above the Schottky layer and adapted to protect the Schottky layer from surface reactions.

6. The structure of claim 5 wherein the GaN termination layer is further a reproducible termination layer, thereby increasing effectiveness of passivation.

7. The structure of claim 5 wherein the GaN termination layer is sufficiently thin to allow electrons to tunnel through the GaN termination layer.

8. The structure of claim 7 wherein the GaN termination is approximately 1-2 nanometers (nm) thick.

9. The structure of claim 1 wherein the contacts comprise a source contact, a gate contact, and a drain contact, further wherein the source, gate, and drain contacts are metallic.

10. The structure of claim 9 wherein a source-drain breakdown voltage is at least one-hundred (100) volts.

11. The structure of claim 1 wherein the transitional layer is deposited on the substrate, the sub-buffer layer is deposited on the transitional layer, and the GaN buffer layer is deposited on the sub-buffer layer.

12. The structure of claim 11 wherein the plurality of epitaxial layers further comprise:

an aluminum nitride Schottky layer deposited on the gallium nitride buffer layer; and

a GaN termination layer deposited on the Schottky layer.

13. A gallium nitride (GaN) transistor structure comprising:

a) a substrate;

b) a plurality of structural epitaxial layers deposited on the substrate and including a GaN buffer layer;

c) a GaN termination layer deposited on the plurality of structural epitaxial layers and adapted to protect the plurality of structural epitaxial layers from surface reactions; and

d) electrical contacts deposited on the GaN termination layer, thereby forming a high electron mobility transistor.

14. The structure of claim 13 wherein the GaN termination layer is further a reproducible termination layer, thereby increasing effectiveness of passivation.

15. The structure of claim 13 wherein the GaN termination layer is sufficiently thin to allow electrons to tunnel through the GaN termination layer.

16. The structure of claim 15 wherein the GaN termination is approximately 1-2 nanometers (nm) thick.

17. The structure of claim 13 wherein the plurality of structural epitaxial layers further comprise a transitional layer deposited above the substrate.

18. The structure of claim 17 wherein the GaN buffer layer is deposited above the transitional layer.

19. The structure of claim 18 wherein the plurality of structural epitaxial layers further comprise a Schottky layer deposited above the GaN buffer layer.

20. The structure of claim 19 wherein the Schottky layer is essentially aluminum gallium nitride.

21. The structure of claim 13 wherein the electrical contacts comprise a source contact, a gate contact, and a drain contact, further wherein the source, gate, and drain contacts are metallic.

22. A method of fabricating a high voltage gallium nitride (GaN) transistor structure comprising:

a) depositing a plurality of structural epitaxial layers on a substrate, comprising:

i) depositing a transitional layer above the substrate;

ii) depositing an aluminum nitride sub-buffer layer above the transitional layer, the sub-buffer layer adapted to prevent electrons

from entering the transitional layer and the substrate during high voltage operation; and

iii) depositing a GaN buffer layer above the sub-buffer layer; and

b) forming electrical contacts on the plurality of structural epitaxial layers, thereby forming a high electron mobility transistor.

23. The method of claim 22 wherein the depositing the plurality of structural epitaxial layers step further comprises depositing a aluminum gallium nitride Schottky layer above the GaN buffer layer.

24. The method of claim 23 wherein the depositing the plurality of structural epitaxial layers step further comprises depositing a GaN termination layer above the Schottky layer.

25. The method of claim 22 wherein the forming electrical contacts step comprises forming a source contact, a gate contact, and a drain contact.